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Abstract: To obtain a resilient and flexible DC grid, reliable means for interfacing its parts operating under different voltage levels must be ensured. This paper proposes bidirectional, isolated, DC–DC converter designed to connect either high/medium voltage bipolar DC grid or two separate high/medium voltage DC grids with another DC grid of similar or different voltage level. In order to achieve galvanic separation among converter stages, while providing redundancy in case of the converter parts malfunction or a DC feeder loss, Scott transformer connection is employed. So far, Scott transformer connection has mostly been used in the railway applications, implying low-frequency operation, in order to obtain two single-phase voltages from a symmetrical three-phase grid. However, its use in the field of the DC–DC conversion has never been analysed in the literature. Further, this paper emphasises operating frequency shift towards the medium frequency range, following the trend of the solid-state transformers which have drawn the attention of both academia and industry worldwide. To control the converter power flow, phase shift control principles are adopted. Consequently, control simplicity is retained, while achieving system complexity reduction. At last, in order to evaluate proposed converter performance, simulation results of a 40 kV/1.5 kV, 10 MW converter are presented, illustrating excellent operating performances.

Nomenclature

V_{in}	converter input voltage
v_{o}	converter output voltage
f	converter operating frequency
T	fundamental switching period ($T = 1/f$)
V_{SM}	MMC submodule voltage
L_{br}	MMC branch inductance
N	number of MMC submodules per branch
m_{T1}	transformer T_1 turns ratio
m_{T2}	transformer T_2 turns ratio
i_{T1}	transformer T_1 primary current
i_{T2}	transformer T_2 primary current
$v_{\text{c}}^{(\text{i})}$	AC voltage generated by the MMC_{i}
P	power
C_{o}	output capacitance
C_{SM}	MMC submodule capacitance
ΔV_{SM}	desired submodule voltage ripple

1 Introduction

Solid-state transformer (SST) concept, primarily foreseen within the AC grids, has also gained a momentum within the DC domain due to the proliferation of renewable energy resources along with growing electrical energy storage and consumption demands. Given that the success of high voltage direct current systems is expected to be replicated within the medium voltage (MV) domain, expansion of the DC grids in the near future is very certain. Flexible and resilient DC grid implies the existence of reliable interfaces among its parts operating under different voltage levels, leading to the conclusion that DC–DC converter can be thought of as its key element. However, certain requirements have to be met in order to support the previous statement, some of which are possibly high step-up/down voltage ratio, high efficiency, isolation due to safety reasons, redundancy, modularity and so on.

Despite the fact that vast amount of research has been conducted in the field of non-isolated DC–DC converters [1–6], this paper focuses exclusively on galvanically isolated structures. Unlike their AC counterparts, isolation stages within DC–DC converters can be designed to operate at an arbitrary frequency. Therefore, bulky low-frequency transformer can be replaced by more compact medium-frequency transformer (MFT). Considering limited voltage blocking capabilities of commercially available semiconductors, reaching as high as 6.5 kV nowadays, dealing with high voltage (HV)/MV at either of a DC–DC converter stages can be quite challenging, thus requiring series connection of power switches [7–10] or converter stages. With the aim of facilitating HV/MV handling, modular multilevel converter (MMC) [11], consisting of series connection of so-called submodules (SMs), can be employed.

MMC-based topologies have been subject to various research projects [12–16]. In [12], MMC-based single-phase (1PH) dual-active bridge (DAB) was thoroughly analysed, whereas the new control method implying sequential insertion of MMC-alike SMs was proposed in [13, 14]. Additionally, MMC-based DC–DC converter operating with sinusoidal currents was reported in [15, 16]. However, sinusoidal current generation requires power semiconductor devices to switch at frequency usually higher compared to the MFT operating (fundamental) frequency, consequently increasing the system losses. Hence, DAB-alike topologies were preferred by the authors of this paper owing to the fact that fundamental frequency switching of power semiconductors can be provided with low control efforts.

Another topic relevant to the scope of this paper is related to transmission lines capacity increase through the conversion of the existing AC power lines into DC [17]. Although the least promising in terms of transmission capacity increase, bipolar DC networks with return (neutral) conductor offer the system redundancy in the case of either of the DC poles outage [18–20]. On these terms, system can continue to operate utilising the neutral conductor, although with reduced power, providing suitable DC–DC converter structure is employed. Figs. 1*a* and *c* present generalised structure of a power converter to be used with the aim of interfacing either HV/MV bipolar DC grid or two separate HV/MV DC grids with a low voltage (LV) DC grid. As suggested by Figs. 1*b* and *d*, system operation, though with reduced power, can be maintained in case either of the DC poles being lost. However, certain system reconfiguration, or operating mode change, might be needed on these terms.

Nevertheless, neither of the topologies proposed in [12–15] were analysed operating within a bipolar grid with neutral

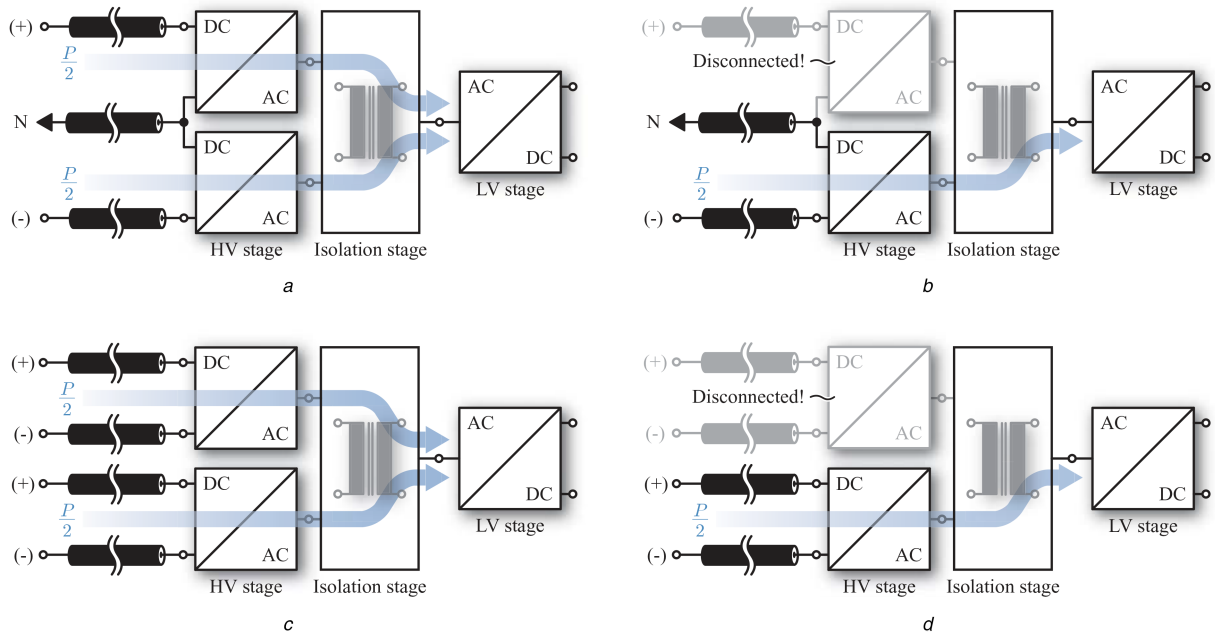


Fig. 1 *Generic structure of a DC–DC converter operating within a bipolar HV/MV grid*

(a) Structure of a converter used to interface HV/MV bipolar DC grid with a LV DC grid. HV/MV stage consists of two converters, providing the possibility of exploiting redundancy principle inherently present within bipolar grids with the neutral conductor, ***(b)*** Converter operation in case one of the voltage poles is lost, ***(c)*** Structure of a converter used to interface two independent HV/MV DC grids of the same voltage level with a LV DC grid, ***(d)*** Converter operation in case one of the DC grids is lost

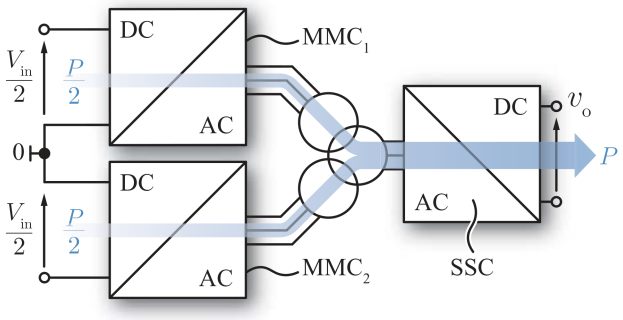


Fig. 2 *Topology employing 3PH three-winding transformer [21]*

conductor nor the possibility of utilising its inherent redundancy property was considered. Topology employing three-phase (3PH) three-winding transformer, with the aim of exploiting the aforementioned redundancy, was proposed in [21]. However, two 3PH MMCs in the HV/MV stage are not irreplaceable in the process of obtaining symmetrical system of 3PH currents in the LV stage.

Scott transformer connection (STC), which has mostly been used within the railway applications so far, can as well be used to obtain symmetrical system of 3PH currents out of two 1PH voltage sources. The use of the MMC in the railway applications was presented in [22–25]. Weiss *et al.* [22] present the possibility to employ the so-called direct MMC in order to provide a single railway line with sinusoidal voltage. On the contrary, the MMC acting as a traction converter was studied in [23]. In order to obtain a railway power conditioner, being in charge of the railway grid STC currents balancing along with harmonics compensation, Song *et al.* [24] combined the STC with two back-to-back 1PH-MMCs. The STC employment has also been reported in [26–29] with the aim of obtaining the unity power factor rectifier. Nevertheless, analysed power, operating frequency and voltage ranges fall significantly below the one being the focus of this paper. Additionally, not one of the references [22–29] has considered combining the MMC with the STC in order to perform the DC–DC conversion, which allows for the operating frequency shift towards medium frequency range, nor has it analysed redundancy principles provided by the existence of two 1PH transformers comprising the STC. It is noteworthy that increase in the STC operating frequency reflects positively upon its size implying the reduced material requirements.

Unlike the topology presented in [21], converter proposed in [30] employed two 1PH MMCs in the HV/MV stage, as well as conventional six-step converter (SSC) in the LV stage. Such a connection was enabled by the unprecedented use of the STC operating in the medium frequency range. The aim of this paper is to provide more thorough analysis of the converter presented in [30], hence its main original contributions can be summarised as

- STC operation in the *medium frequency* range is proposed
- Bidirectional high-power *DC–DC* converter utilising the STC is proposed
- *Redundancy* principles, increasing flexibility and reliability of the proposed topology, are demonstrated

This paper is organised as follows. Section 2 includes a detailed description of the proposed topology followed by the explanation of operating principles in both normal and de-rated modes. Converter design guidelines are presented within Section 3. Method employed to control the converter power flow was covered within Section 4, whereas Section 5 provides simulation results obtained in PLECS, analysis on the converter semiconductor losses and their comparison with the solution being adopted as a point of reference.

2 Proposed topology

2.1 Derivation

Fig. 2 depicts the state-of-the-art topology proposed in [21]. Two 3PH MMCs were used in the HV/MV stage with the aim of interfacing the voltage across converter's DC terminals, whereas conventional SSC was employed in the LV stage.

STC, presented in Fig. 3 along with its voltage phasor diagram, has already been used for more than a century in the line frequency applications. It is known for providing two 1PH sinusoidal voltage sources out of a single 3PH voltage source, which is widely used in the railway networks even nowadays. T_2 Secondary (S)-winding is divided into two parts, both having number of turns equal to $N/2$. In order to ensure proper STC operation, T_1 S-winding number of turns has to be set as $N\sqrt{3}/2$. Consequently, with identical number of Primary (P)-winding turns, turns ratios relation is

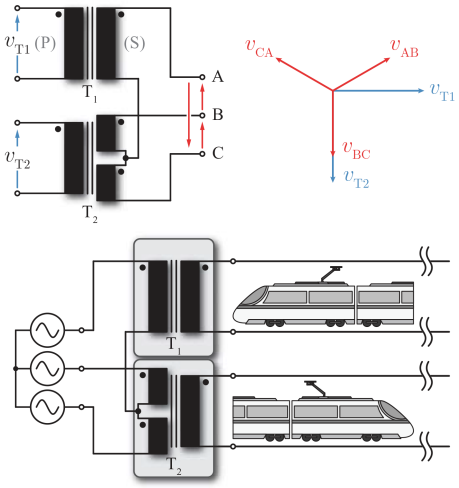


Fig. 3 *STC with its voltage phasor diagram (upper); the most common use of the STC (lower)*

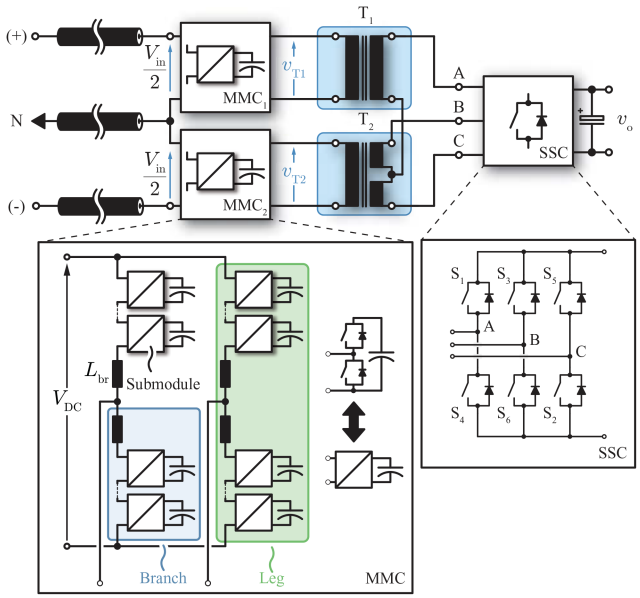


Fig. 4 *Proposed topology consisting of two series connected MMCs in the HV/MV stage (since bipolar grid with neutral conductor is available), STC and conventional SSC in the LV stage*

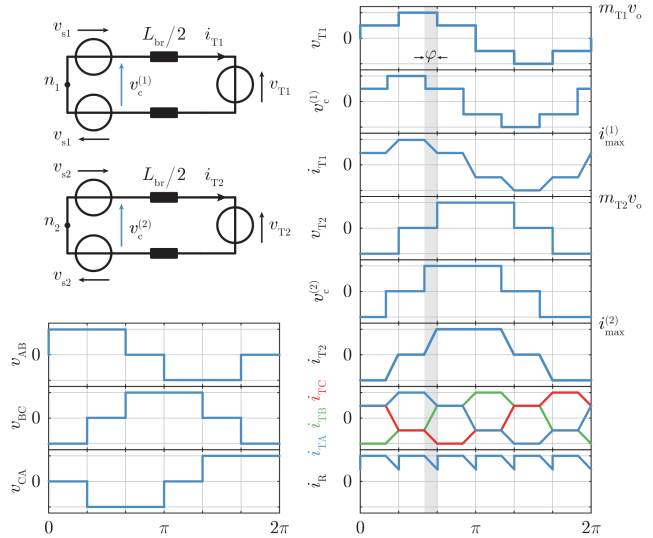


Fig. 5 *Equivalent circuits of two MMCs connected to T_1 and T_2, respectively, along with the voltage/current waveforms relevant for the converter analysis*

$m_{T1} = 2m_{T2}/\sqrt{3}$. Nonetheless, instead of driving the STC with sinusoidal voltages, fundamental switching with square-wave voltages is utilised in this work. SSC being connected to T_1 and T_2 S-windings results in square-wave-alike voltages across their P-windings. Therefore, to interface voltages created across both transformers' P-windings, 1PH MMCs are used, as presented in Fig. 4. Hence, employment of the STC instead of the 3PH three-winding transformer leads to the reduction of MMC branches number by the factor of 1/3 compared to the topology presented in [21]. System redundancy can be exploited, though with certain system modifications which are to be outlined in the upcoming subsection. Furthermore, the STC operation is not constrained to the low operating frequencies (mains frequency) considering different nature of its employment. Therefore, operating frequency shift towards medium frequency range can be achieved resulting in the system volume and weight reduction.

2.2 Operating principles

Fig. 4 presents the proposed converter consisting of two series connected MMCs in the HV/MV stage and the SSC in the LV stage. It is noteworthy that in the case of LV replacement with HV/MV, the SSC can be replaced with any suitable structure. To interface HV/MV grid, both MMCs use half-bridge (HB) SMs. Number of HB SMs depends on available HV/MV and voltage class of semiconductors employed within the MMCs. SSC operates with square-wave voltages (at medium operating frequency, e.g. a few kHz) with the aim of minimising switching losses. It can be shown that instantaneous voltages across T_1 and T_2 P-windings (v_{T1} and v_{T2}, respectively) correspond to the combination of the LV side quantities, according to the following equations:

$$v_{T1} = m_{T1}\frac{v_{AB} - v_{CA}}{2} \tag{1}$$

$$v_{T2} = m_{T2}v_{BC} \tag{2}$$

Further, it can be seen from Fig. 5 that voltages v_{T1} and v_{T2} differ in shape. However, MMC provides the possibility of an arbitrary voltage waveform generation, as long as energy balances within the converter are maintained. Fig. 5 depicts equivalent circuits of both MMCs connected to their associated transformers. With the appropriate voltage waveforms generated by the MMCs, energy transfer can be controlled by adjusting the phase shift (φ) between the observed MMC AC voltage ($v_c^{(i)}$) and its associated transformer EMF (v_{Ti}). Consequently, proposed configuration represents phase-modulated structure, which relies on the control principles introduced with the appearance of the DAB [31]. It is noteworthy that a MMC AC voltage amplitude should match the amplitude of its associated transformer EMF, therefore $\hat{v}_c^{(i)} = \hat{v}_{Ti}$.

Fig. 5 presents idealised voltage waveforms to be generated by the MMCs, as well as currents flowing through both transformers' P-windings. Based on expressions (1) and (2), peak voltages $\hat{v}_{T1}$ and $\hat{v}_{T2}$ can be calculated. If output voltage reference value was denoted by v_o, then $\hat{v}_{T1} = m_{T1}v_o$ and $\hat{v}_{T2} = m_{T2}v_o$. By analysing the waveforms given by Fig. 5, power at which the energies are flowing through T_1 and T_2 can be derived (3) and (4). It is noteworthy that $P_{T1} = P_{T2}$ if turns ratio relation given above holds, while $\varphi_1 = \varphi_2$. According to Fig. 5, adjacent legs within either of the MMCs have to generate two voltages of the same amplitude, however in counterphase. This means that the observed MMC legs can be controlled in the complementary manner. In other words, a leg AC pole reference voltage v_{si} will be used with the opposite sign for the adjacent leg within the same MMC. In (3) and (4), L_Σ accounts for the sum of a MMC branch inductance and its associated transformer leakage inductance. However, throughout the following sections, transformers' leakage inductances are assumed negligible with respect to the MMC branch inductance

$$P_{T1} = \frac{m_{T1}^2 V_o^2}{\omega L_\Sigma}\varphi_1\left(\frac{1}{2} - \frac{3\varphi_1}{8\pi}\right) \tag{3}$$

$$P_{T_2} = \frac{m_{T_2}^2 V_o^2}{\omega L_\Sigma} \varphi_2 \left(\frac{2}{3} - \frac{\varphi_2}{2\pi} \right) \tag{4}$$

If either of the DC poles or MMCs happens to be lost, de-rated operation of the system can be ensured providing certain modifications are performed, according to Fig. 6. On these terms, MMC connected to the faulty DC pole gets disconnected from the circuit, whereas the other one continues its operation, however with differently generated voltage waveforms. Considering that symmetrical system of 3PH currents cannot be created in the LV side by virtue of a single MMC, the system is forced to operate as the 1PH DAB. Such a configuration is already well known, whereas control method proposed in [32] can be employed. Upcoming sections will expand on this subject.

3 System design

Table 1 summarises ratings of the system observed for the purposes of providing thorough insight into design guidelines and simulation. In the forthcoming analysis, it will be assumed that proposed converter interfaces either a bipolar HV/MV DC grid or two separate DC grids of the same voltage level with a LV DC grid. Additionally, converter design is conducted assuming converter operation without faults (normal operating conditions), which can easily be proven as critical from the system design point of view.

3.1 Number of MMC SMs

It is assumed that both MMCs accept equal voltages at their DC terminals. Number of SM to be employed within a MMC depends on the available HV/MV across its DC terminals, as well on the voltage class of semiconductor devices to be employed. Considering MVDC voltage levels and desire to have a reasonable number of SMs, the use of 3.3 kV IGBT modules was considered by this paper (any other voltage level can as well be considered). Hence, with typical DC-link voltage of around 1.8 kV for a single SM, $N = 12$ SMs are needed.

3.2 Transformers turns ratios

Prior to commencing any further analyses, it is worth noting that voltage across both transformers P-windings has to match voltages impressed into the system by both MMCs with the aim of maintaining fundamental switching frequency of all semiconductor devices within the converter. Moreover, voltage across T_2 P-winding equals $\sqrt{3}/2$ times T_1 P-winding voltage due to the relationship between the STC turns ratios. T_1 turns ratio will be determined such that the voltage generated across its P-winding matches the voltage impressed into the system by the MMC_1, hence (5) can be written

$$m_{T1} = \frac{V_{in}}{2V_o} \tag{5}$$

However, using the turns ratios relationship originally defined by the STC might cause the mismatch between AC voltage created by the MMC_2 and voltage across T_2 P-winding, considering that the number of inserted SMs must be a round number within both MMCs (if fundamental switching frequency is to be retained under all operating conditions). However, a whole set of fractions (ξ) being quite close to $\sqrt{3}/2$, as listed in Table 2, exists.

If maximum number of SMs being inserted within a branch of the MMC_2 was denoted as $\hat{n}_{n2} = \alpha N$, as presented in Fig. 7, peak voltage across its AC terminals $\hat{v}_2$ can be calculated as

$$\hat{v}_2 = (2\alpha - 1)\frac{V_{in}}{2} \tag{6}$$

Given that T_2 P-winding peak voltage ($\hat{v}_2$) equals $\xi V_{in}/2$ (providing coefficient ξ is used instead of $\sqrt{3}/2$), relationship

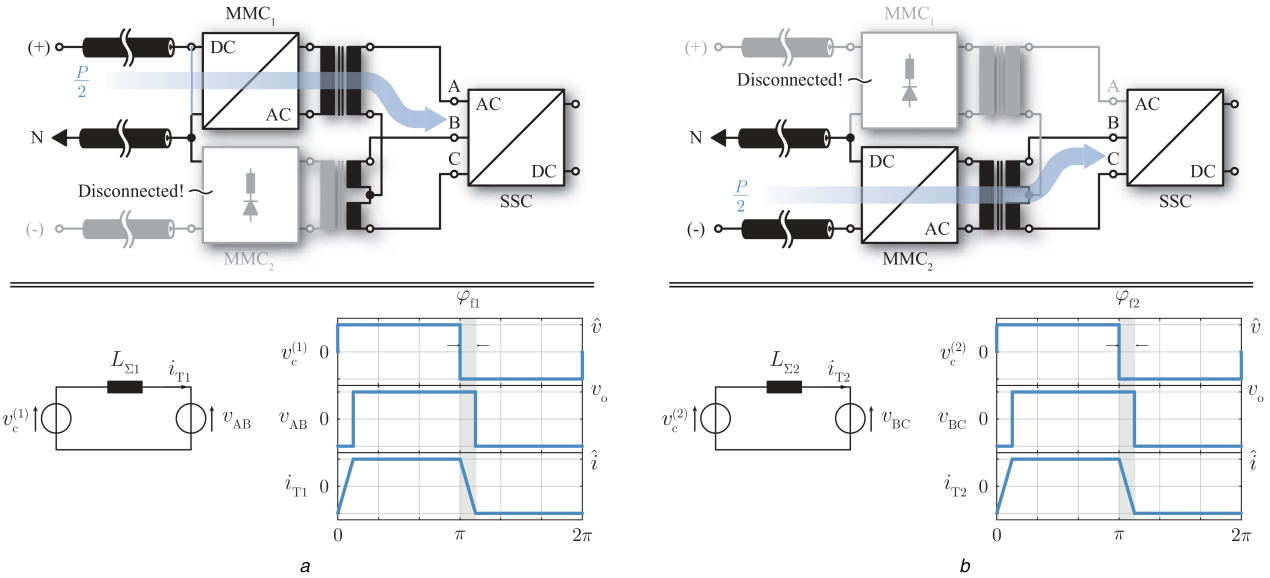


Fig. 6 *Proposed topology reconfiguration in case either of the DC poles is lost*

(a) Negative DC pole was lost. T_2 P-winding can be considered open circuit providing MMC_2 gets isolated from the rest of the circuit. Therefore, system can continue to operate as the 1PH DAB, ***(b)*** Positive DC pole was lost. T_1 P-winding can be considered open circuit providing MMC_1 gets isolated from the rest of the circuit. Therefore, system can continue to operate as the 1PH DAB

Table 1 Analysed system parameters

Parameter	Value
input voltage	40 kV
output voltage	1.5 kV
rated power	10 MW
system operating frequency	1 kHz

Table 2 Coefficients possibly used instead of $\sqrt{3}/2$

Fraction (ξ)	Float	α	No. of SMs employed ($n \in N$)
4/5	0.8	9/10	$4 \cdot 5n$
5/6	0.833	11/12	$4 \cdot 3n$
6/7	0.857	13/14	$4 \cdot 7n$
7/8	0.875	15/16	$4 \cdot 4n$

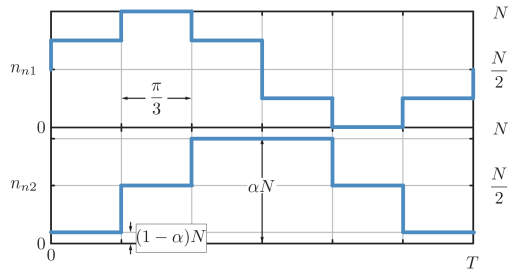


Fig. 7 *Number of inserted SMs within both MMCs*

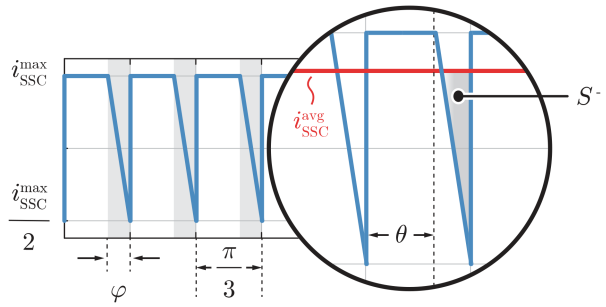


Fig. 8 *Idealised SSC output current*

between a fraction being utilised instead of the original ratio defined by the STC and coefficient α can be established

$$\xi = (2\alpha - 1) \tag{7}$$

Therefore, fraction of total SMs number, within the MMC_2, to be inserted in order to match T_2 peak voltage can be determined as

$$\alpha = \frac{\xi + 1}{2} \tag{8}$$

According to the fourth column of Table 2, if number of MMC SMs is set as $N = 12$, T_2 turns ratio is to be chosen as

$$m_{T2} = \frac{5}{6} m_{T1} \tag{9}$$

What comes out as a direct consequence of such turns ratios choice is uneven split between powers at which the energies are transferred through T_1 and T_2. However, as shown in the upcoming sections, this issue can be addressed by means of a suitable control algorithm.

3.3 MMC branch inductor design

Considering inevitable presence of branch inductors within both MMCs, double role can be assigned to them. On one hand, branch inductors are used to limit the MMC common-mode current ripple originating from voltage oscillations across MMC SMs. On the other hand, MMC branch inductors can be used to control the converter power transfer since a MMC equivalent inductance seen from its associated transformer P-winding equals its branch inductance.

Of course, this statement holds providing transformers' leakage inductances can be considered negligible compared to MMCs branch inductances. Therefore, for a given system rated power P_{nom}, operating frequency f and nominal phase angle φ_{nom}, branch inductance can be calculated according to (3) or (4), leading to

$$L_{br} = \frac{2m_{T1}V_o^2}{\omega P_{nom}} \varphi_1 \left(\frac{1}{2} - \frac{3\varphi_1}{8\pi} \right) \tag{10}$$

Adopting nominal phase angle as $\varphi_{nom} = 10°$, along with the use of parameters provided in Table 1 and above-derived transformers turns ratios relation, leads to the arm inductance being set as $L_{br} = 1$ mH.

3.4 SMs capacitor design

The purpose of transformers turns ratios determination according to Section 3.2 was to provide the conditions for both MMCs fundamental frequency switching, meaning that every power switch operates at the MFT operating frequency. Fundamental period is observed through several subintervals, whereas each one of them causes MMC SMs to acquire certain amount of charge leading to the voltage ripple across its' capacitors. However, this analysis falls out of this paper's scope. MMC capacitances were calculated according to (11), so that SMs' voltage ripple (ΔV_{SM}) remains between $\pm 1.25\%$ of its rated voltage, leading to $C_{SM} = 4.25$ mF. Consequently, amount of energy installed within the converter per one kW equals $E_c/P = 56.9$ J/kW

$$C_{SM} \geq \frac{4\pi - 3\varphi_{nom}}{3\omega^2 L_{br} \Delta V_{SM}} \varphi_{nom} V_{in} \tag{11}$$

3.5 LV stage capacitor bank design

Capacitor bank in the LV stage can be designed according to a desired output voltage ripple, which originates from the SSC output current ripple ideally occurring at six times operating frequency of the converter. Fig. 8 presents the idealised waveform of the SSC output current. The area causing the output capacitor voltage to drop can be labelled with S^-, as depicted in Fig. 8. Hence, (12) can be easily derived

$$\begin{aligned} \Delta V_o &= \frac{S^-}{\omega C_o} \\ &= \frac{I_{max}}{\omega C_o} \left| \int_\theta^{\pi/3} \left[1 - \frac{\omega t - (\pi/3) + \varphi}{2\varphi} - \left(1 - \frac{3\varphi}{4\pi} \right) \right] \mathrm{d}(\omega t) \right| \\ &= I_{max} \left| \frac{4\varphi\pi^2 + 12\varphi^2\pi - 9\varphi^3}{16\omega C_o \pi^2} \right| \end{aligned} \tag{12}$$

According to Fig. 5, maximum value of the SSC output current can be effortlessly calculated. For the output voltage peak-to-peak ripple being expressed as a percentage of the reference value (α), the output capacitance can be set according to (13), which gives $C_o \simeq 2.65$ mF should $\alpha = 1.5\%$ be the requirement to meet

$$C_o \geq \frac{m_{T1}^2 \varphi_{nom}^2 \left| (4\pi^2 + 12\varphi_{nom}\pi - 9\varphi_{nom}^2) \right|}{16\omega^2 L_{br} \alpha \pi^2} \tag{13}$$

Table 3 summarises the values of all passive components used for the proposed topology simulation.

Table 3 Values of passive components used for simulation purposes

Parameter	Value
number of MMC SMs	12
system operating frequency	1 kHz
MMC branch inductance	1 mH
MMC SMs capacitance	4.25 mF
output capacitance	2.65 mF

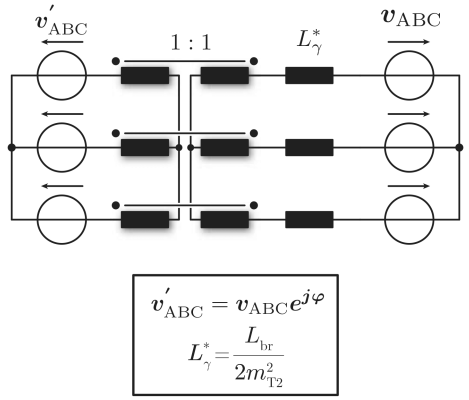


Fig. 9 *3PH DAB equivalence of the proposed converter*

4 System control

4.1 Equivalent 3PH-DAB model

Henceforth, LV stage will be referred to as output, whereas HV/MV will be referred to as input stage. In order to set a solid basis for system control related discussions, behaviour of the LV side currents should be investigated. Ampere-turns balance equations can be set for both transformers, leading to

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} m_{T1} & 0 \\ \frac{-m_{T1}}{2} & m_{T2} \\ \frac{-m_{T1}}{2} & -m_{T2} \end{bmatrix} \begin{bmatrix} i_{T1} \\ i_{T2} \end{bmatrix} \tag{14}$$

According to Fig. 5, transformers' primary side currents can be described with the following equation:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{T1} \\ i_{T2} \end{bmatrix} = \frac{1}{L_{\mathrm{br}}}\begin{bmatrix} v_c^{(1)} - m_{T1}\dfrac{V_{AB} - V_{CA}}{2} \\ v_c^{(2)} - m_{T2}V_{BC} \end{bmatrix} \tag{15}$$

Since the LV stage consists of three phases, its current behaviour can be observed in the $\alpha\beta$ plane (16). It is of interest to observe the SSC currents changes during the converter operating period, therefore (16) needs to be differentiated, leading to the system of equations (17) and (18)

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} \tag{16}$$

$$\frac{\mathrm{d}i_\alpha}{\mathrm{d}t} = \frac{2v_c^{(1)}m_{T1}}{2L_{\mathrm{br}}} - m_{T1}^2\frac{3V_\alpha^{ABC}}{2L_{\mathrm{br}}} \tag{17}$$

$$\frac{\mathrm{d}i_\beta}{\mathrm{d}t} = \frac{2\sqrt{3}}{3L_{\mathrm{br}}}\left(v_c^{(2)}m_{T2} - V_\beta^{ABC}\sqrt{3}m_{T2}^2\right) \tag{18}$$

It would be quite convenient if α and β components of the input stage voltages appeared in (17) and (18). However, input stage consists of two 1PH transformers, hence excluding the possibility for $\alpha\beta$ transformation of its quantities. However, voltages to be generated by both MMCs ($v_c^{(1)}$ and $v_c^{(2)}$) represent the certain combinations of the LV quantities, which enables their observation through virtual voltage system $\vec{v}'_{ABC}$ having the amplitude of the LV stage phase voltages, however leading by the phase angle φ ($\vec{v}'_{ABC} = \vec{v}_{ABC}\mathrm{e}^{\mathrm{j}\varphi}$). Consequently, voltages $v_c^{(1)}$ and $v_c^{(2)}$ can be expressed as

$$v_c^{(1)} = m_{T1}\frac{V'_{AB} - V'_{CA}}{2} \tag{19}$$

$$v_c^{(2)} = m_{T2}V'_{BC} \tag{20}$$

Assuming that $m_{T1} = 2m_{T2}/\sqrt{3}$ and substituting (19) and (20) into (17) and (18) leads to the simplified system of equations describing LV stage α and β components (21) and (22). Therefore, LV stage current vector can be calculated (23)

$$\begin{aligned} \frac{\mathrm{d}i_\alpha}{\mathrm{d}t} &= 2m_{T1}^2\frac{V'_{AB} - V'_{CA}}{2L_{\mathrm{br}}} - m_{T1}^2\frac{3V_\alpha^{ABC}}{2L_{\mathrm{br}}} \\ &= \frac{3m_{T1}^2}{2L_{\mathrm{br}}}(V'_\alpha - V_\alpha) \\ &= \frac{2m_{T2}^2}{L_{\mathrm{br}}}(V'_\alpha - V_\alpha) \end{aligned} \tag{21}$$

$$\begin{aligned} \frac{\mathrm{d}i_\beta}{\mathrm{d}t} &= \frac{2m_{T2}^2}{L_{\mathrm{br}}}\frac{V'_{BC} - V_{BC}}{\sqrt{3}} - m_{T1}^2\frac{3V_\alpha^{ABC}}{2L_{\mathrm{br}}} \\ &= \frac{2m_{T2}^2}{L_{\mathrm{br}}}(V'_\beta - V_\beta) \end{aligned} \tag{22}$$

$$\begin{aligned} \frac{\mathrm{d}\boldsymbol{i}_{\alpha\beta}}{\mathrm{d}t} &= \frac{\mathrm{d}}{\mathrm{d}t}(i_\alpha + ji_\beta) \\ &= \frac{2m_{T2}^2}{L_{\mathrm{br}}}[V'_\alpha + jV_\beta - (V'_\alpha + jV_\beta)] \\ &= \frac{2m_{T2}^2}{L_{\mathrm{br}}}[\boldsymbol{V}'_{\alpha\beta} - \boldsymbol{V}_{\alpha\beta}] \end{aligned} \tag{23}$$

Current vector equation (23) indicates that the proposed topology can be observed through its equivalent 3PH-DAB model, presented in Fig. 9. The circuit consists of the ideal 3PH transformer, with turns ratio equal to one, equivalent inductance $L_\gamma^* = (L_{\mathrm{br}}/2m_{T2}^2)$ and two conventional SSCs being modelled by the ideal 3PH voltage sources. In order to get the equivalent inductance, MMC branch inductance has to be divided by the square of T_2 turns ratio, which indicates that the equivalent circuit represents the converter observed from the LV stage. Moreover, seen from the LV stage, MMCs operate in parallel which is confirmed by the fact that branch inductance has to be divided by two in order to acquire the equivalent inductance L_γ^*.

To confirm the validity of the circuit presented in Fig. 9, power at which the energy is transferred from P to the S winding should match the power of the original circuit. It is known that 3PH-DAB power can be calculated as

$$P_{\mathrm{DAB}}^{(3)} = \frac{3\hat{V}^2}{\omega L_\gamma^*}\varphi\left(\frac{1}{2} - \frac{3\varphi}{8\pi}\right) \tag{24}$$

In the above equation, $\hat{V}$ refers to the amplitude of transformer phase voltage, which equals $\hat{V} = (2/3)\hat{V}_{ABC}$. Considering that voltage sources $\vec{v}_{ABC}$ have the amplitude equal to the original system output voltage, one can conclude that $\hat{V} = (2/3)v_{\mathrm{o}}$. Substitution of $\hat{V}$ into (24) along with the use of expression for the equivalent inductance L_γ^*, leads to

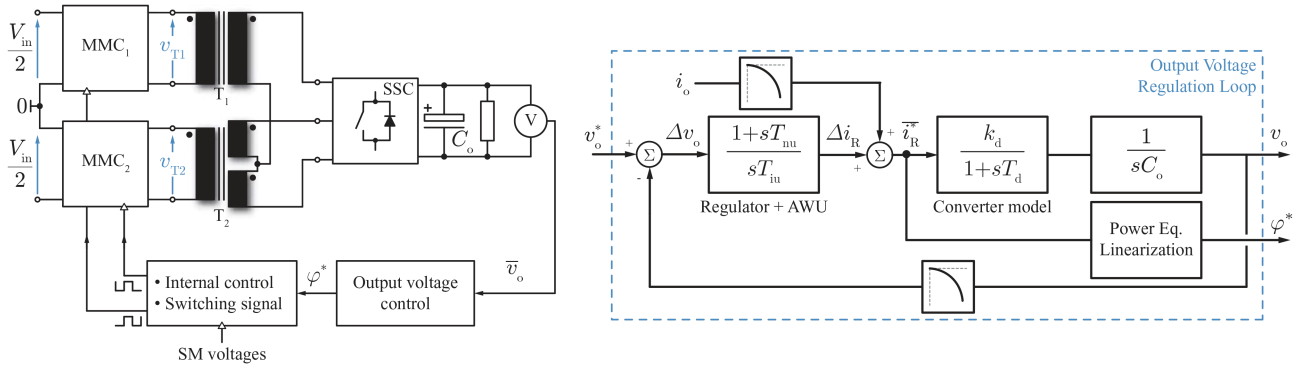


Fig. 10 *Output voltage control block diagram (left); output voltage regulation loop (right)*

$$\begin{aligned} P_{\mathrm{DAB}}^{(3)} &= 3\frac{(2v_{\mathrm{o}}/3)^2}{\omega(L_{\mathrm{br}}/2m_{T2}^2)}\varphi\left(\frac{1}{2}-\frac{3\varphi}{8\pi}\right) \\ &= 2\frac{4v_{\mathrm{o}}^2 m_{T2}^2}{3\omega L_{\mathrm{br}}}\varphi\left(\frac{1}{2}-\frac{3\varphi}{8\pi}\right) \\ &= 2P_{\mathrm{MMC}}^{(1)} \\ &= P_{\Sigma} \end{aligned} \tag{25}$$

The above expression suggests that the 3PH-DAB equivalent matches the original system in terms of the LV side behaviour as well as the power transfer. Therefore, 3PH-DAB control algorithms already presented in the literature [33–35] can be applied to the system being the subject of this paper. Additionally, even if transformers turns ratios relationship originally defined by the STC is violated, precision of the above results should not be severely hindered. According to Table 2, fractions possibly utilised instead of $\sqrt{3}/2$ indeed result in a certain transformers power transfers mismatch, however, it will be shown that this issue can easily be addressed by means of a suitable control tactics.

4.2 Output voltage control under normal operating conditions

Output voltage control was performed according to Fig. 10, with the aim of maintaining the output voltage mean value ($\bar{v}_{\mathrm{o}}$) equal to the reference defined in Table 1. Seen from the LV side, SSC can be perceived as an ideal current source owing to the fact that the DAB-based circuits output current does not depend on its output voltage. Therefore, in order to regulate the output voltage, SSC output current mean value ($\bar{i}_{\mathrm{R}}$) should be adjusted. However, variable to be affected within the DAB-alike systems is the phase shift between relevant voltage waveforms. Therefore, phase angle (φ) information needs to be extracted from the SSC output current reference ($\bar{i}_{\mathrm{R}}^{*}$).

Observing (3) and (4), one can connect SSC output current mean value with HV/MV quantities, however, this would result in the need for solving non-linear equations. Linearisation of power curves given by (3) and (4) around desired operating angle can be performed. It can be shown that this will not significantly hinder the precision of obtained results. Ultimately, voltage regulator will compensate for the errors introduced by the aforementioned linearisation. If linearisation point was chosen as $\varphi_{\mathrm{lin}} = \pi/6$, system power equation can be rewritten as

$$P_{\mathrm{o}} = \frac{7\zeta V_{\mathrm{in}} v_{\mathrm{o}} m_{T1}}{16\omega L_{\Sigma}}\varphi \tag{26}$$

Given that output power can be perceived as a product of the SSC output current mean value and output voltage, phase angle information can be extracted from the SSC output current reference based on (27). Moreover, owing to the fact that the whole converter can be modelled with an ideal current source seen from the LV side, load current (i_{o}) can be used as a feed-forward variable. What goes in favour of such a statement is that SSC mean output current value equals the load current once the steady state is reached

$$\varphi^{*} = \frac{16\omega L_{\Sigma}}{7\zeta V_{\mathrm{in}} m_{T1}}\bar{i}_{\mathrm{R}}^{*} \tag{27}$$

Although very convenient, the use of the same phase angle to control both transformers power flow can result in the system power distribution inequality due to several reasons. Firstly, number of secondary turns differs for T_1 and T_2, consequently resulting in different secondary impedances. Further, if the above-presented method of determining transformers' turns ratios is used ($m_{T1} \neq 2m_{T2}/\sqrt{3}$), power transfers defined by (3) and (4) are not equal. Therefore, additional control loop has to be applied upon the converters phase shifts φ_1 and φ_2. Assuming stiff HV/MV, mismatch in converters mean powers results in the neutral conductor current average value being different than zero. Hence, this variable can be used with aim of bringing T_1 and T_2 powers to the same level. According to Fig. 11, a difference between MMCs input currents mean values gets compared to zero. Thereafter, this value gets passed to the PI controller (W_{c}), whose output can be perceived as a power correction applied to both transformers (ΔP). However, to convert the PI controller output into phase angle corrections, power equations (3) and (4) need to be linearised, leading to (28) and (29). Both regulation loops parameters can be found in Table 4. It is noteworthy that transformer power corrections are expected to be very modest, otherwise system design should be reconsidered, hence controller W_{c} can be slower compared to the output voltage regulator, which can be confirmed according to Table 4

$$\Delta\varphi_1 = \frac{16\omega L_{\Sigma}}{7\hat{v}_{T1}^2}\Delta P \tag{28}$$

$$\Delta\varphi_2 = \frac{12\omega L_{\Sigma}}{7\hat{v}_{T2}^2}\Delta P \tag{29}$$

4.3 MMC balancing

In order to keep both MMCs voltages within a predefined range, idea presented in [32] was used. Depending on the voltage distribution within a branch observed at the beginning of a switching period kT, along with the information on electric charge acquired during the previous switching period, different gate signals are distributed to both MMCs SMs. However, detailed analysis falls out of this paper's scope.

5 Simulation results

5.1 Normal operating conditions

Proposed high-power DC–DC converter was modelled and simulated in PLECS. In order to test converter operating performances, load power profile depicted in Fig. 12 was used. Fig. 13 presents converter operating waveforms during the time interval $T_{\mathrm{sim}} = 5$ s.

According to the figure below, converter successfully responds to the power requirements imposed by the defined load profile,

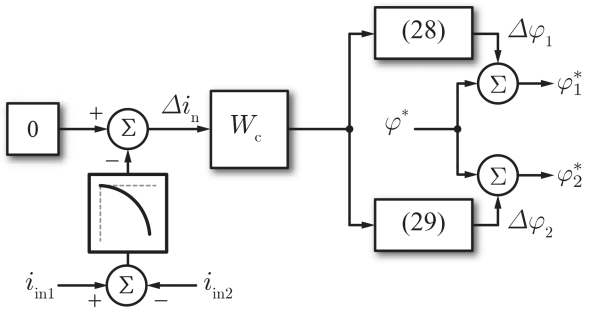


Fig. 11 *Transformers' power matching control implementation*

Table 4 Control loops parameters

Controller	Parameter	Value
output voltage	proportional gain (k_{p1})	6.67
	integral gain (k_{i1})	1.1
	sampling time (T_{s1})	0.5 ms
power balancing	proportional gain (k_{p2})	714.16
	integral gain (k_{i2})	628.32
	sampling time (T_{s2})	5 ms

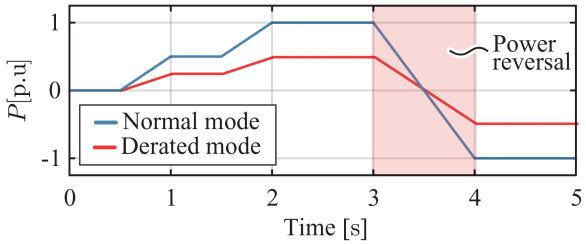


Fig. 12 *Load power profile normalised with respect to the rated power of the converter*

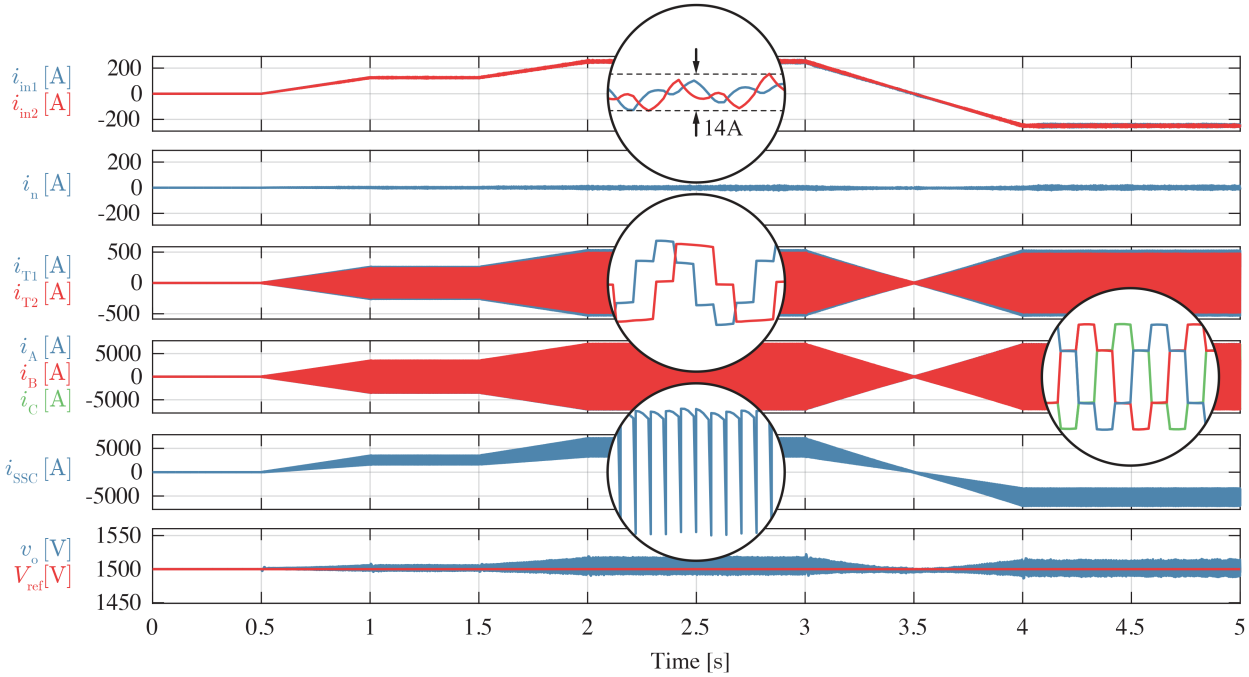


Fig. 13 *Proposed topology operating waveforms during the time interval $T_{sim} = 5\,s$*

which can be concluded based on the shape of both MMCs input currents (i_{in1} and i_{in2}, respectively). These two currents differ only in terms of ripple, which originates from the oscillations of the MMC SMs voltage, thus neutral conductor current (i_n) does not contain any average component. It is noteworthy that, even though the load power demand changes, abrupt phase angle changes must not be allowed within the DAB-based converters as it would cause LV stage currents unbalance [33, 35]. At time instant $T = 3\,s$, converter gradually reverses its power over the interval $\Delta T = 0.5\,s$, as can be seen from the topmost plot.

To confirm the correspondence between idealised waveforms, presented in Fig. 5, and the ones obtained by means of simulations, Fig. 14 presents both transformers currents, the SSC output current along with the output voltage, during three operating cycles. Both

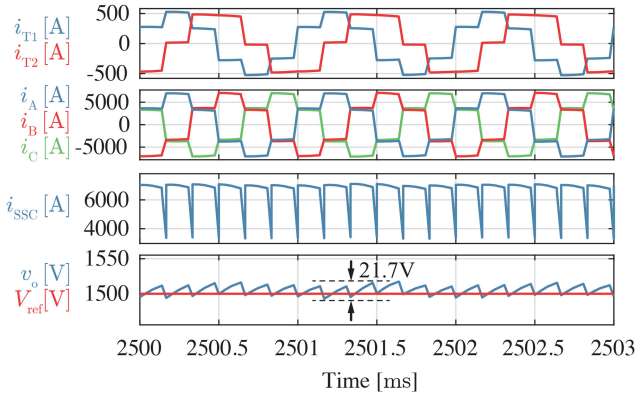


Fig. 14 *Converter operation during three fundamental cycles. Correspondence between the idealised waveforms presented in Fig. 5 and the ones obtained in simulations can be observed. The SSC output current consists of the mean value along with the ripple, occurring predominantly at six times converter operating frequency, being superimposed*

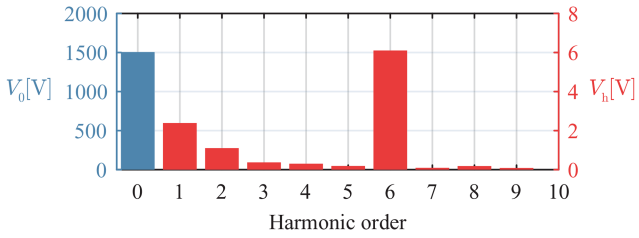


Fig. 15 *Output voltage spectrum. Owing to the presented sizing of the output capacitor, harmonics in the output voltage fall significantly below the mean value, which corresponds to the reference value. Therefore, the output voltage mean value was labelled with blue, whereas the values of all the other harmonics should be observed on the right-hand side axis coloured in red*

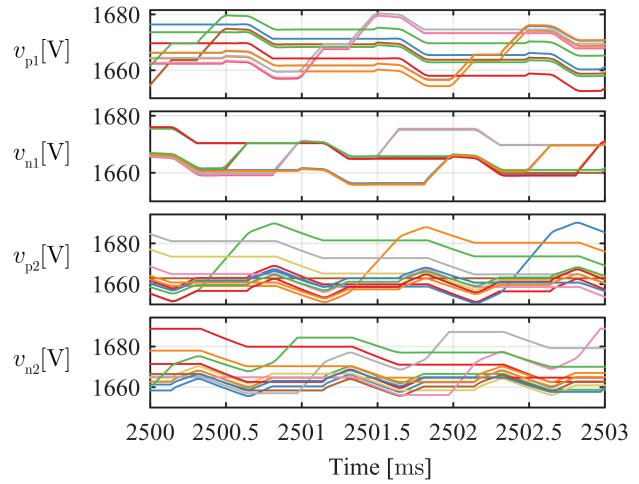


Fig. 16 *MMCs capacitor voltages during three fundamental periods*

T_1 and T_2 P-winding currents (i_{T1} and i_{T2}, respectively) correspond to the idealised waveforms presented in Fig. 5. As expected, the SSC output current (i_{SSC}) consists of the mean value along with the ripple occurring at six times converter operating frequency being superimposed, whereas the output voltage consists of the mean value along with the ripple originating from the SSC current oscillations. Also, the shape of the LV stage AC currents (i_A, i_B and i_C) corresponds to the one observed in the conventional 3PH DAB.

Fig. 15 presents the output voltage spectrum with the frequency axis being normalised with respect to the converter operating frequency. Given that the output voltage mean value significantly exceeds the other harmonics being present in the output voltage, it is presented by the blue bar. All the other harmonics can be read from the right-hand side axis, being coloured in red. It is easy to see that the dominant harmonic in the output voltage occurs at six times operating frequency of the converter, which is expected owing to the correlation between the proposed topology and the 3PH DAB. Notwithstanding, a set of lower order harmonics can as well be observed. These can be considered a consequence of various factors such as resistances, which are not considered during the idealised waveforms derivation, non-ideal T_1 and T_2 turns ratio relation and so on. Nonetheless, harmonics occurring at multiples of six times the operating frequency remain the most emphasised, although all of the harmonics can be considered negligible compared to the output voltage average.

Fig. 16 presents voltages across MMC_1 (v_{p1}, v_{n1}) and MMC_2 (v_{p2}, v_{n2}) leg 'A' SMs. Subscripts 'p' and 'n' denote upper and lower MMC branch, respectively. It can be seen that mean value of a SM voltage equals ~1.67 kV ($V_{SM} = V_{in}/2N$), as expected. Peak-to-peak ripple of a SM voltage equals ~36 V, thus matching the criteria presented in Section 3.4.

To benchmark the operation of the proposed topology, semiconductor loss comparison against the structure containing two 3PH DABs in the ISOP configuration, as presented in Fig. 17, was carried out. Both converters operate with parameters provided in Table 1. It is noteworthy that in order to conduct the efficiency analysis of two different solutions, both of them have to be completely known. In other words, two separate designs would have to be carried out, which falls out of this paper's scope. Therefore, only semiconductor losses are calculated and compared. To realise the switch of a desired voltage rating, either of the DABs from the figure below consists of the series connection of IGBTs on the HV/MV side. Hence, a switch can be realised by connecting 20 Infineon FZ400R17KE4 ($V_{ce,s} = 1.7$ kV, $I_c = 400$ A) IGBTs in series. On the LV side though, semiconductor devices need to be connected in parallel in order to meet the topology current handling requirements, which can be achieved by connecting five ABB 5SNE 0800E330100 ($V_{ce,s} = 3.3$ kV, $I_c = 800$ A) IGBTs in parallel per every switch.

To follow the above-described design procedure of the topology depicted in Fig. 4, number of the MMC SMs per branch on the HV/MV side was set as $N = 12$, meaning that 3.3 kV IGBT modules can be used with the aim of interfacing the bipolar grid. Infineon FF4450R33T3E3 ($V_{ce,s} = 3.3$ kV, $I_c = 450$ A) was selected as a module of choice. On the LV side however, semiconductor devices need to be connected in parallel in order to meet the current requirements. Therefore, five HiPak ABB 5SNA 1800E330400 ($V_{ce,s} = 3.3$ kV, $I_c = 1800$ A) IGBTs need to be connected in parallel to obtain the switch of the desired ratings. Please keep in mind that such a choice of semiconductor devices within both converters can be considered exemplary and different selections might results in different results comparison-wise.

Fig. 18 presents semiconductor losses, expressed as a percentage of the converter operating power, for both of the solutions presented in Figs. 4 and 17. Seen from the LV side, the topology presented in Fig. 4 behaves identically to the 3PH DAB, therefore all the conveniences regarding the semiconductors zero-voltage switching (ZVS)/zero-current switching (ZCS) are retained [31]. However, on the HV/MV side, the presence of the common-mode current within the MMCs branches hinders the ZVS/ZCS performance, which results in slightly increased semiconductor losses of the proposed topology with respect to the one presented in Fig. 17. However, if one were to calculate the total efficiency of the system, an additional amount of power losses would be observed on the HV/MV side of the topology depicted in Fig. 17 owing to the need for the snubbing circuitry due to the series connection of the semiconductor devices. Unlike the topology from Fig. 4, two high-voltage capacitors would have to be mounted within the terminals of the bipolar grid, in order to filter the higher order harmonics, occurring at six times multiples of the DAB operating frequency, from the DAB DC-link currents. Last but not least, design of two 1PH MFT with the aim of ensuring the same LV side behaviour can be considered easier compared to the design of a two 3PH MFT.

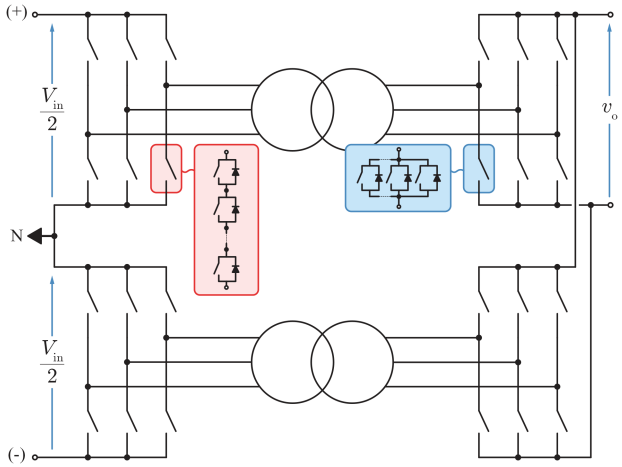


Fig. 17 *Exemplary solution used to benchmark the operation of the proposed converter. It consists of two 3PH DABs in the series output parallel (ISOP) configuration, consequently providing the system redundancy in case either of the DC poles or HV/MV converters happens to fail*

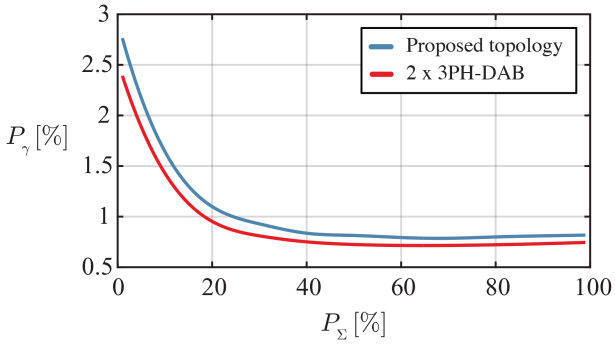
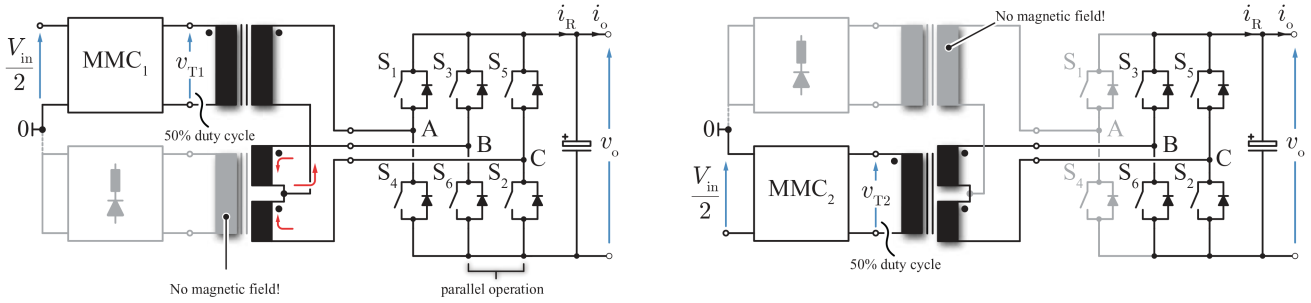


Fig. 18 *Semiconductor losses comparison between the proposed topology and the one consisting of two DABs in the ISOP configuration*



a *b*

Fig. 19 *Converter operation under faulty operating conditions*
(a) Negative DC pole outage, ***(b)*** Positive DC pole outage

5.2 De-rated operation mode

Main convenience provided by a bipolar DC grid lies within its redundancy in case either of the DC poles happens to be lost. On these terms, as already stated, the MMC being connected to the faulty DC pole gets isolated from the circuit whereas the other one continues to supply the load with half the rated power. However, due to the space limitations, transition from normal to de-rated operating mode will not be analysed in this paper. In other words, steady-state operation in the de-rated mode is presented. Additionally, if either of the DC poles is lost, 3PH voltage system cannot be created at the LV side, therefore converter operates as the 1PH-DAB.

Fig. 19*a* depicts the way that converter operates in case negative DC pole is lost. Since 1PH voltages need to be generated at both converter stages, there is a possibility of operating the SSC legs B and C in parallel. On these terms, T_1 secondary current splits in two equal parts between the legs B and C. Operation of two SSC legs, being a part of the 3PH DAB, in parallel has already been studied with the aim of performing advanced triangular modulation schemes [36]. Nevertheless, in this paper, the SSC supplies T_1 P-winding with 50% duty cycle square-wave voltages despite the other modulation methods being feasible to implement. To control the power flow, phase shift control principles are retained meaning that the control block diagram presented in Fig. 10 remains valid.

Fig. 19*b* depicts the way that converter operates in case positive DC pole is lost. Switches S_1 and S_4 are kept in the off state, therefore isolating T_1 from the rest of the circuit. SSC legs B and C supply T_2 P-winding with 50% duty cycle square-wave voltages, meaning that control principles presented above can provide satisfactory results.

Figs. 20*a* and *b* present converter operation during three fundamental cycles, under half of the converter rated load (nominal load in the de-rated mode), in the case of negative and positive DC pole outage, respectively. To test the converter performance in the de-rated mode, load power profile presented in Fig. 12 was used. Please notice that the converter can supply the LV stage with half the rated power on these terms. In both cases, converter operates as the 1PH DAB, the outcome of which is the output voltage and current consisting of the mean value and the ripple occurring at twice the fundamental frequency superimposed. One can notice that, regardless of the analysed fault, transformer connected to

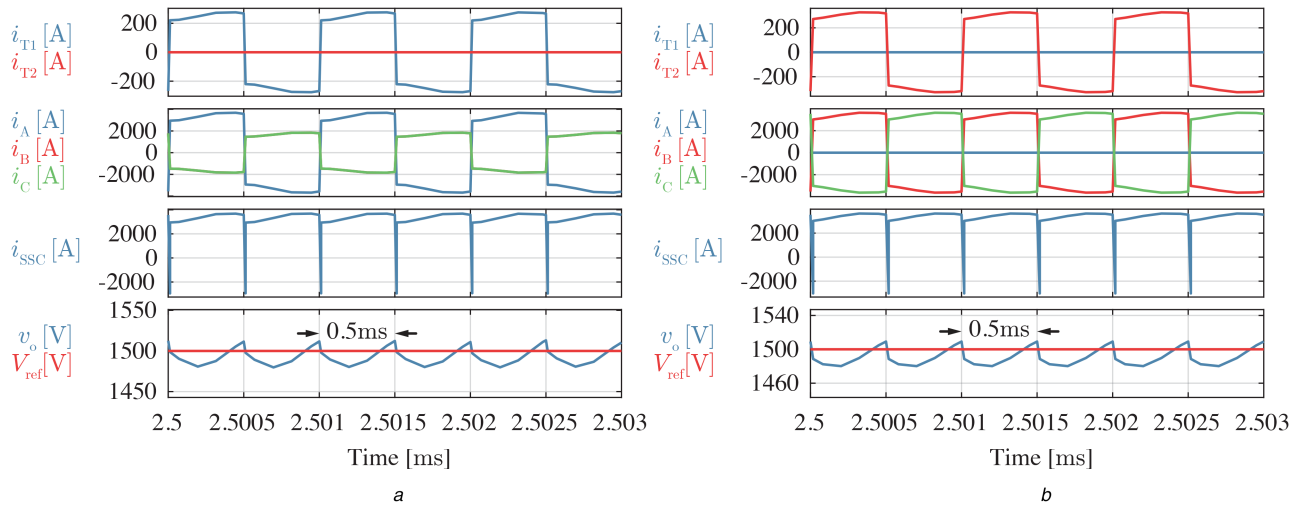


Fig. 20 *Converter operation in the de-rated mode during three fundamental cycles*

(a) Converter operating waveforms during three fundamental cycles in the case of negative DC pole outage, ***(b)*** Converter operating waveforms during three fundamental cycles in the case of positive DC pole outage

malfunctioned MMC has zero P-winding voltage and current in the ideal case. Nevertheless, should a certain mismatch in the switching instants of the SSC legs B and C, from Fig. 19*a*, exist, a short pulse of voltage across the T_1 P-winding would not create significant currents owing to the presence of the branch inductors within the MMC_2. Once again, abrupt phase angle changes need to be treated with care, otherwise converter being in operation can suffer significant current offsets, possibly leading to a trip or, in the worst case scenario, exposing the converter to the operating areas being unsafe.

6 Conclusion

This paper proposed a novel MMC-based, bidirectional, high-power DC–DC converter utilising STC, operating in the medium frequency range for the first time, as means of isolation between HV/MV and LV stages. With the aim of providing the possibility to exploit the amenities offered by the presence of the neutral conductor, two 1PH transformers are used. Nevertheless, proper form AC voltages have to be generated by the MMCs. Consequently, system complexity reduction is achieved, while maintaining redundancy principle. If any of the voltage poles happens to be lost, converter can continue to operate in the de-rated mode, however as the 1PH DAB, meaning that certain, not too complicated though, circuit configuration changes have to be performed. Seen from the LV stage, this topology behaves as same as conventional 3PH DAB. Therefore, all LV stage soft-switching properties are retained. Internal MMC control algorithm was developed with the aim of enabling every IGBT within both MMC to operate with fundamental switching frequency, therefore minimising the switching losses. Semiconductor losses were calculated and compared with the solution incorporating two 3PH DABs in the ISOP configuration. Owing to the presence of the common-mode current within two MMCs employed on the HV/MV side, semiconductor losses are slightly increased with respect to the solution used as a point of reference. However, the proposed topology offers a set of advantages such as the absence of high-voltage capacitors in the DC-link, removal of the snubbing circuits used in case semiconductor devices are connected in series (with the aim of meeting the converter voltage requirements), redundancy in case some of the semiconductor devices happen to fail and so on. Design of the STC MFT, as well the utilisation of various modulation methods, were left for the future research given the STC unprecedented use in the high-power medium frequency DC–DC conversion. Additionally, in case unidirectional power converter is to be obtained, the SSC in the LV stage can be replaced with a diode rectifier, resulting in the topology operating in a different manner. However, future publications are going to expand further on this topic.

7 Acknowledgments

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